

Silicon NPN Power Transistors

2SD1446

DESCRIPTION

- With TO-220Fa package
- High DC current gain
- High collector to base voltage V_{CBO}
- DARLINGTON

APPLICATIONS

- For power amplification

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

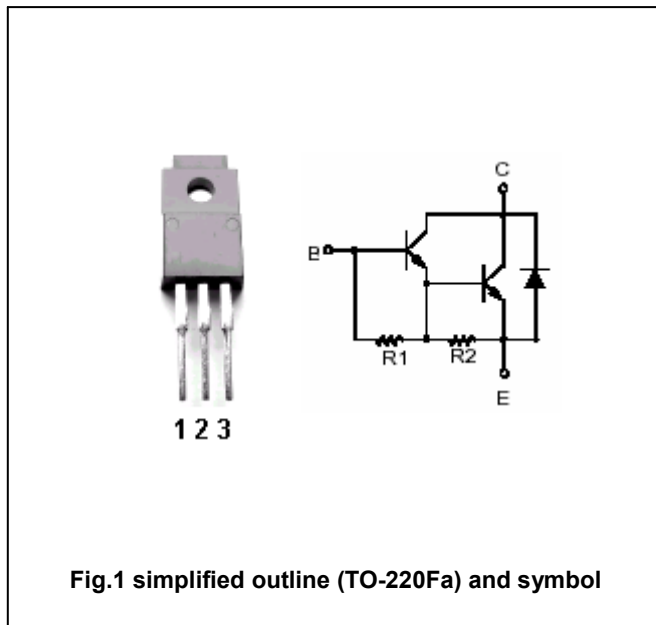


Fig.1 simplified outline (TO-220Fa) and symbol

Absolute maximum ratings($T_a=25^\circ C$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	500	V
V_{CEO}	Collector -emitter voltage	Open base	400	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		6	A
I_{CP}	Collector current peak		10	A
P_C	Collector power dissipation	$T_C=25^\circ C$	40	W
		$T_a=25^\circ C$	2.0	
T_j	Junction temperature		150	$^\circ C$
T_{stg}	Storage temperature		-55~150	$^\circ C$

Silicon NPN Power Transistors

2SD1446

CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =0.1A; I _C =0	5			V
V _{CEO(SUS)}	Collector-emitter sustaining voltage	I _C =2A; L=10mH	400			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =3A; I _B =0.06A			1.5	V
V _{BEsat}	Base-emitter saturation voltage	I _C =3A; I _B =0.06A			2.5	V
I _{CBO}	Collector cut-off current	V _{CB} =350V; I _E =0			100	μA
h _{FE}	DC current gain	I _C =2A; V _{CE} =2V	500			
f _T	Transition frequency	I _C =1A; V _{CE} =10V;		15		MHz

Silicon NPN Power Transistors

2SD1446

PACKAGE OUTLINE

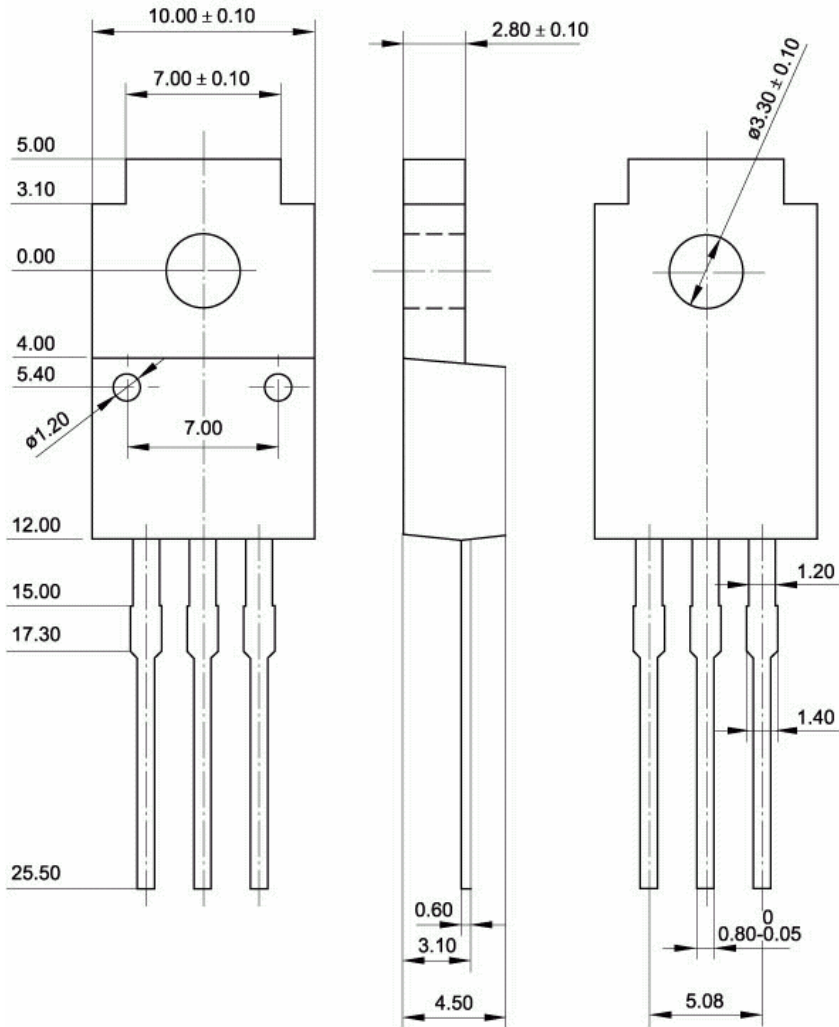


Fig.2 Outline dimensions (unindicated tolerance: ± 0.15 mm)