MOSFET Power Transistor

BLF245

65V / 6A

DATASHEET

OEM – Philips

Source: Philips Data Handbook SC19a 1998

VHF power MOS transistor BLF245

FEATURES

- High power gain
- Low noise figure
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

Matched gate-source voltage (V_{GS}) groups are available on request.

PIN CONFIGURATION

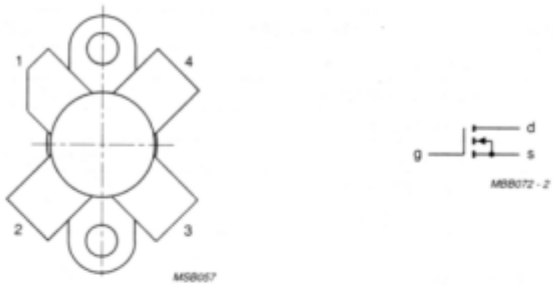

Fig.1 Simplified outline and symbol.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	30	> 13	> 50

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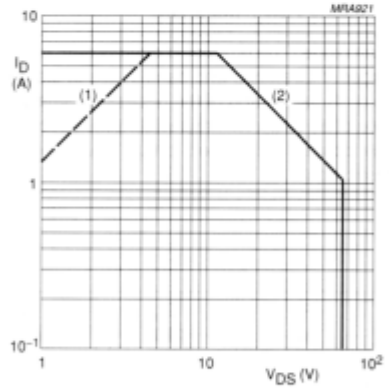
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	V_{GS} = 0	–	65	V
$\pm V_{GS}$	gate-source voltage	V_{DS} = 0	–	20	V
I_D	DC drain current		–	6	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	68	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

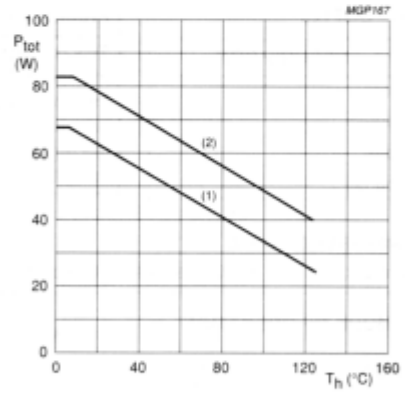
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 68 W	2.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 68 W	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2	mA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	µA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched devices	I_D = 10 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.5 A; V_{DS} = 10 V	1.2	1.9	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1.5 A; V_{GS} = 10 V	–	0.4	0.75	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	10	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	125	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	75	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	7	–	pF
F	noise figure (see Fig.14)	input and output power matched for: I_D = 1 A; V_{DS} = 28 V; P_L = 30 W; R1 = 1 kΩ; T_h = 25 °C; f = 175 MHz	–	2	–	dB